Vortex86SX

32-BIT x86 Embedded SoC

Brief Datasheet (v1.000)

CONTENTS

1 Overview

Vortex86SX is the x86 SoC (System on Chip) with 0.13 micron process and ultra low power consumption design (less than 1 watt). This comprehensive SoC has been integrated with rich features, such as various I/O (RS-232, Parallel, USB and GPIO), BIOS, WatchDog Timer, Power Management, MTBF counter, LoC (LAN on Chip),JTAG etc., into a 27x27 mm, 581-pin BGA packing single chip.

The Vortex86SX is compatible with Win CE, Linux and DOS. It integrates 32KB write through direct map L1 cache, 16-bit ISA bus, PCI Rev. 2.1 32-bit bus interface at 33 MHz, SDRAM, DDR2, ROM controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), SPI (Serial Peripheral Interface), Fast Ethernet MAC, FIFO UART, USB2.0 Host and IDE controller into a System-on-Chip (SoC) design.

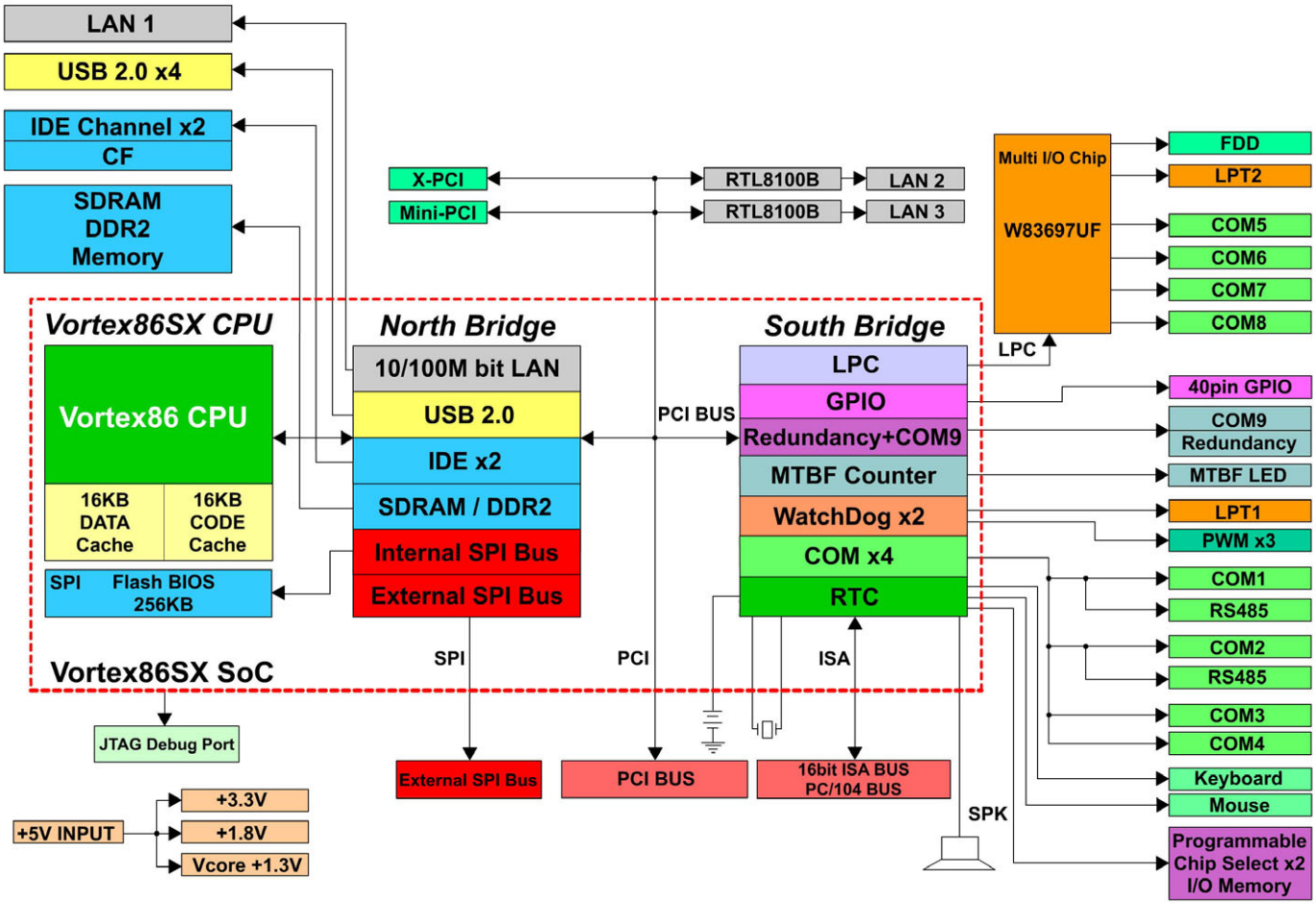
Furthermore, this outstanding Vortex86SX SoC can not only meet the requirements of embedded applications, such as Electronics Billboard, Firewall Router, Industrial Single-Board-Computers, Receipt Printer Controller, Thin Client PC, Auto Vehicle Locator, Finger Print Identification, Web Camera Thin Server, RS232-to-TCP Transmitter. but also can meet the critical temperature demand, spanning from -40 to +85 ℃.

2 Features

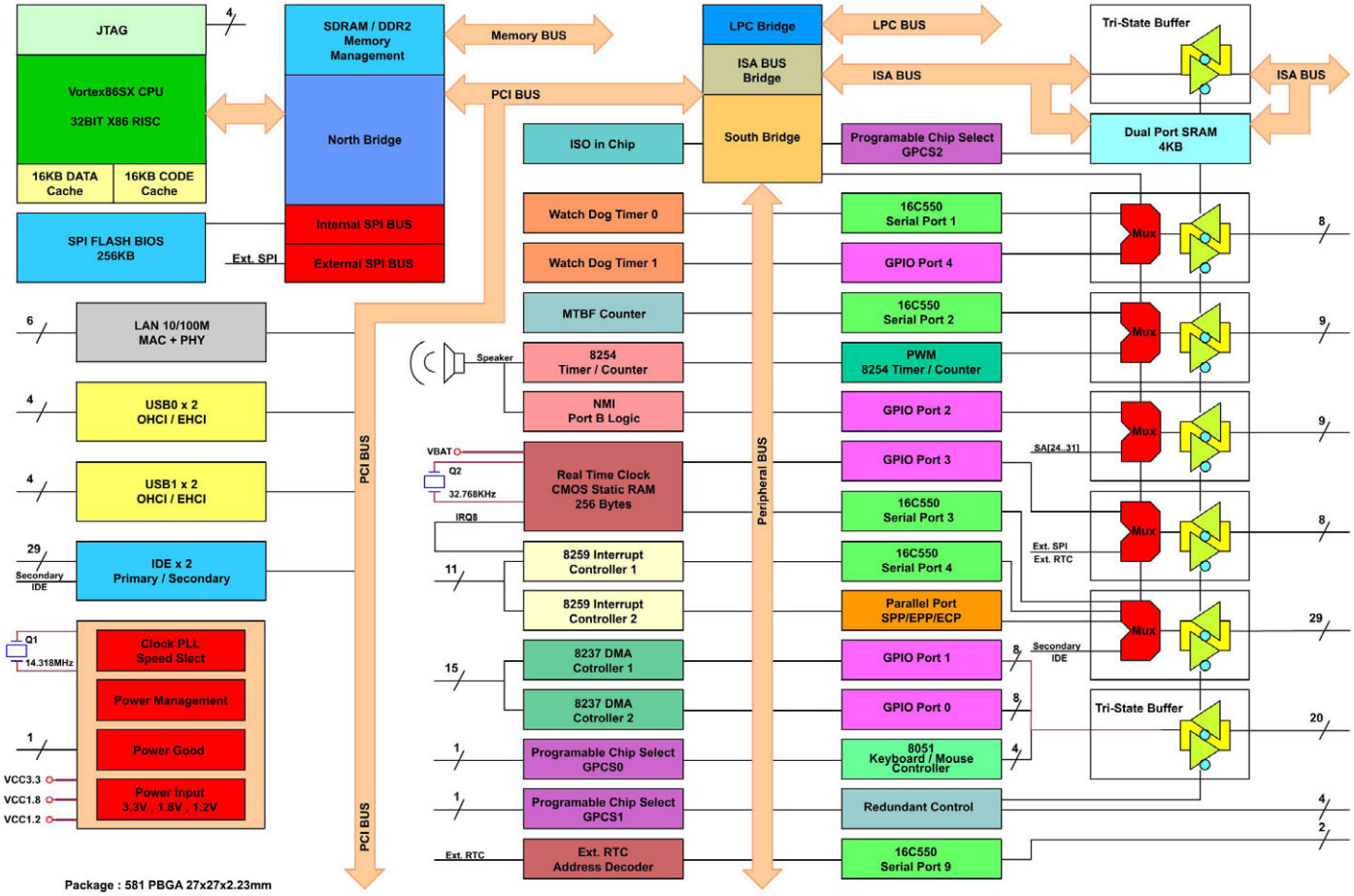
- ***x86 Processor Core***
  - 6 stage pipe-line
- ***Embedded I/D Separated L1 Cache***
  - 16K I-Cache, 16K D-Cache
- ***SDRAM/DDRII Control Interface***
  - 16 bits data bus
  - Support DLL for clock phase auto-adjustion
  - SDRAM support up to 133MHz
  - SDRAM support up to 128Mbytes
  - DDRII support up to 166MHz
  - DDRII support up to 256Mbytes
- ***IDE Controller***
  - Support 2 channels Ultra-DMA 100 (Disk x 4)
- ***LPC (Low Pin Count) Bus Interface***
  - Support 2 programable registers to decode LPC address
- ***MAC Controller x 1***
- ***PCI Control Interface***
  - Up to 3 sets PCI master device
  - 3.3V I/O
- ***ISA Bus Interface***
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
- ***DMA Controller***
- ***Interrupt Controller***
- ***Counter/Timers***
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- ***MTBF Counter***
- ***Real Time Clock***
  - Below 2uA power comsuption on Internal Mode (Estimation Value)
- ***FIFO UART Port x 5 (5 sets COM Port)***
  - Compatible with 16C550/16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1/COM2
  - Port 80h output data could be sent to COM1 by software programming
- ***Parallel Port x 1***
  - Support SPP/EPP/ECP mode
- ***General Chip Selector***
  - 2 sets extended Chip Selector
  - I/O-map or Memory-map could be configurable
  - I/O Addressing: From 2 byte to 64K byte
  - Memory Address: From 512 byte to 4G Byte
- ***General Programmable I/O***
  - Supports 40 dedicated programmable I/O pins
  - Each GPIO pin can be individually configured to be an input/output pin
- ***USB 2.0 Host Support***
  - Supports HS, FS and LS
  - 4 port
- ***PS/2 Keyboard and Mouse Interface Support***
  - Compatible with 8042 controller
- ***Redundant System Support***
- ***Speaker out***
- ***Embedded 256KB Flash***
  - For BIOS storage
  - The Flash could be disable & use external Flash ROM
- ***JTAG Interface supported for S.W. debugging***
- ***Input clock***
  - 14.318MHz
  - 32.768KHz
- ***Output clock***
  - 24 MHz
  - 25 MHz
- ***Operating Voltage Range***
  - Core voltage: 1.2 V ~ 1.4V
  - I/O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- ***Operating temperature***
  - -40℃ ~ 85℃
- ***Package Type***
  - 27x27mm, 581 ball BGA

3 Block Diagram

3.1 System Block Diagram



3.2 Function Block Diagram (Internal)

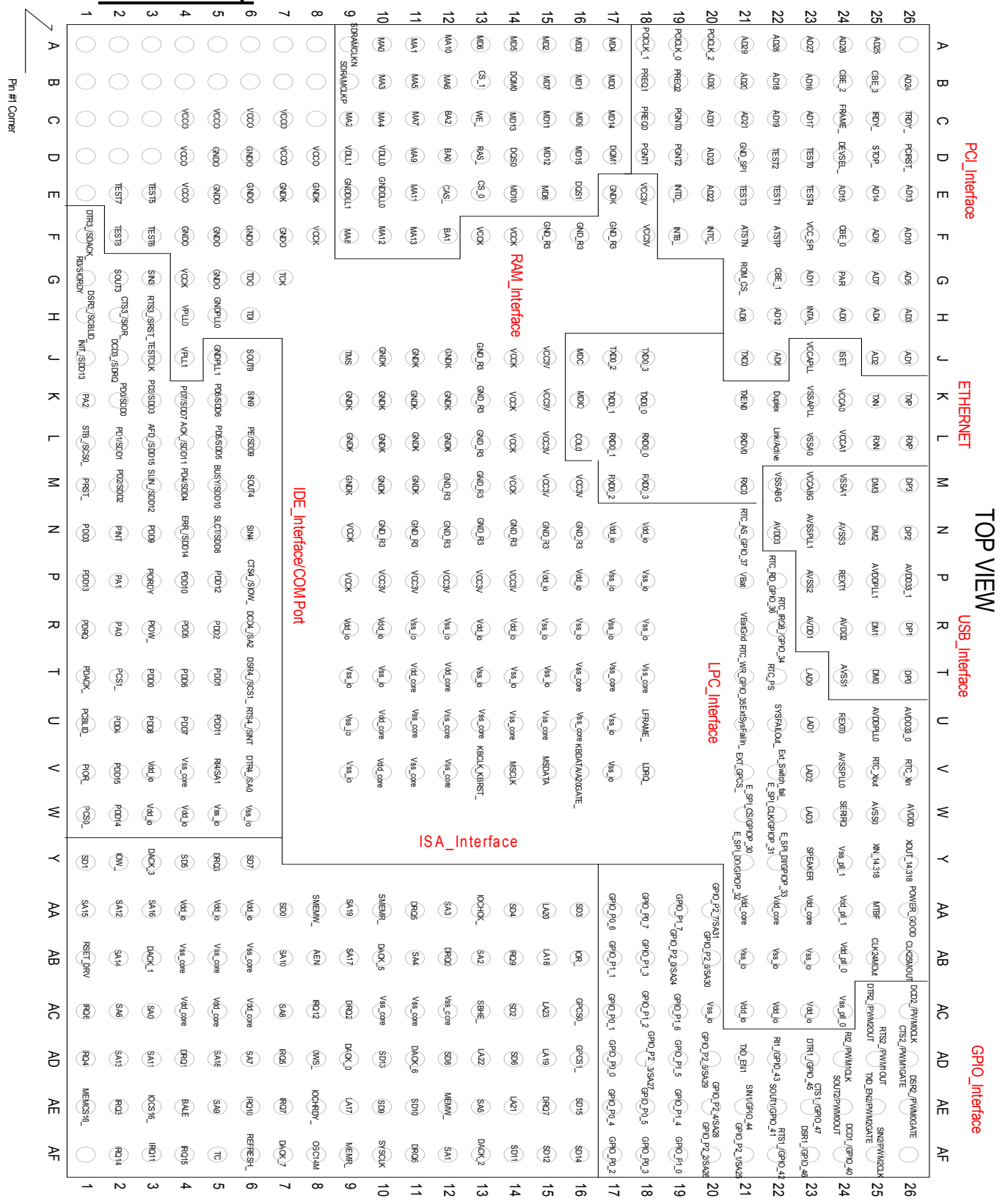


3.3 PCI Device List

Device#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	
IDSEL	AD11	AD12	AD13	AD14	AD15			AD18	AD19		AD21	AD22	AD23		
Function 0	NB	PCI SLOT1	PCI SLOT2	PCI SLOT3	PCI SLOT4			SB	MAC		USB0 OHCI	USB1 OHCI	IDE		
Function 1											USB0 EHCI	USB1 EHCI			

4 PIN Function List

4.1 BGA Ball Map



4.2 Signal Description

This chapter provides a detailed description of Vortex86SX signals. A signal with the symbol "_n" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

OD Output pin with open-drain

I/O Bi-directional Input/Output pin

- **System (7 PINs)**

PIN No.	Symbol	Type	Description
AA26	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The Vortex86SX uses this signal to generate reset sequence for the system.
AB26	25MOUT	O	***25MHz Clock output.***
Y26	XOUT_14.318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
Y25	XIN_14.318	I	***Crystal-in.*** 14.318MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
AA25	MTBF		***MTBF Flag output.***
AB25	CLK24MOUT	O	***24MHz Clock output***
Y23	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker

- **SDRAM /DDRII Interface (44 PINs)**

PIN No.	Symbol	Type	Description
B9	SDRAMCLK	O	***Clock output.*** This pin provides the fundamental timing for the SDRAM /DDR controller.
A9	SDRAMCLKN	O	***Clock output.*** This pin provides the fundamental timing for the SDRAM /DDR controller.
D13	RAS_	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the SDRAM/DDR clock. This signal also allows row access and pre-charge.
E12	CAS_	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the SDRAM/DDR clock. This signal also allows column access and pre-charge.
C13	WE_	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
B13, E13	CS_[1:0]	O	***Chip Select CS[1:0].*** These two pins activate the SDRAM devices. First Bank of SDRAM accepts any command when the CS0_n pin is active low. Second Bank of SDRAM accepts any command when the CS1_n pin is active low. For DDRII, only CS0_n activates the DDR device.
B14, D17	DQM[1:0]	O	***Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
E16, D14	DQS[1:0]	I/O	***Data Strobe DQS[1:0 for DDR only.*** Output with write data, input with the read data for source synchronous operation.

F12, D12	BA[1:0]/Strap[17:16]	O	***Bank Address BA[1:0].*** These pins are connected to SDRAM/DDR as bank address pins. ***Strap[17:16].*** Memory Select, Default pull high. Strap[17] Strap[16] DRAM Select 0 0 SDRAM 0 1 Reserved 1 0 DDR 1 1 DDRII (Default)
C12	BA[2]	O	***Bank Address [2].*** These pins are connected to SDRAM/DDR as bank address pins.
D16, C17, C14, D15, C15, E14, C16, E15, B15, A13, A14, A17, A16, A15, B16, B17	MD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the SDRAM/DDR data bus.
A10	MA[0]	O	***Memory Address MA[0].*** Normally, these pins are used as the row and column address for SDRAM/DDR.
A11	MA[1]/Strap[1]	O	***Memory Address MA[1].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[1].*** Pull it high to enable GPIO2. Default pull high. Pull it low to enable Address[31:24].
C9	MA[2]	O	***Memory Address MA[2].*** Normally, these pins are used as the row and column address for SDRAM/DDR.
B10	MA[3] /Strap[3]	O	***Memory Address MA[3].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[3].*** PLL_TEST_OUT_EN_, Default pull low. Pull it high to enable PLL_TEST_OUT_EN_. Pull it low to disable PLL_TEST_OUT_EN_.
C10	MA[4] /Strap[4]	O	***Memory Address MA[4].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[4]/[10].*** SDRAM/DDR clock, Default pull high. Strap[10] Strap[4] SDRAM clock 0 0 100MHz 0 1 133MHz *(Internal default)* 1 0 166MHz 1 1 200MHz
C11,B12,B11	MA[7:5]/Strap[7:5]	I/O	***Memory Address MA[7:5].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[7:5] / CPU Clock*** ***3b'000 / Bypass mode*** ***3b'001 / SYN_DISABLE_ (CPU clock same to SDRAM Clock)*** ***3b'010 / 233MHz*** ***3b'011 / 266MHz*** ***3b'100 / 300MHz (Internal default)*** ***3b'101 / 333MHz*** ***3b'110 / 366MHz*** ***3b'111 / 400MHz***
F9	MA[8]/Strap[8]	I/O	***Memory Address MA[8].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[8].*** Pull it high to enable Vortex86SX JTAG. Default internal pull-high.

D11	MA[9]/Strap[9]	I/O	***Memory Address MA[9].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[9].*** Pulled low: 33 PINS is for IDE2. Pulled high: 33 PINS is for COM3/4 and Parallel Port. Default internal pull-high.
A12	MA[10]/Strap[10]	I/O	***Memory Address MA[10].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[4]/[10].*** SDRAM/DDR clock, Default pull low. Strap[10] Strap[4] Memory clock 0 0 100MHz 0 1 133MHz *(Internal default)* 1 0 166MHz 1 1 200MHz
E11	MA[11]/Strap[11]	I/O	***Memory Address MA[11].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[11].*** Pulled low is Internal RTC. Default internal pull-low. Pulled high is External RTC
F11,F10	MA[13:12]/ Strap[13:12]	I/O	***Memory Address MA[13:12].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[13:12].*** 00 : flash-8bits 01 : flash-16bits 11 : Internal SPI. Default internal pull-high.

- **USB 0, 1, 2, 3 (10 PINs)**

PIN No.	Symbol	Type	Description
T26 T25	USB0_DP USB0_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
R26 R25	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
N26 N25	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
M26 M25	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
U26	REXT[0]:	I	Universal Serial Bus Controller 0 External Reference Resistance. 510Ω ±10%
P26	REXT[1]:	I	Universal Serial Bus Controller 1 External Reference Resistance. 510Ω ±10%

- **PCI Bus Interface (56 PINs)**

PIN No.	Symbol	Type	Description
B19, B18, C18	PREQ_[2:0]	I	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.
D19, D18 ,C19	PGNT_[2:0]	O	***PCI Bus Grant.*** These signals are the PCI bus grant output signals generated by the internal PCI arbiter.
D26	PCIRST_	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
A19 A18 A20	PCICLK_0 PCICLK_1 PCICLK_2	O	***PCI Clock Output.*** This clock is used by all of the Vortex86SX logic that is in the PCI clock domain.

C20, B20, A21 A22, A23, A24, A25, B26, D20, E20, C21, B21, C22, B22, C23, B23, E24, E25, E26, H22, G23, F26, F25, H21, G25, J22, G26, H25, H26, J25, J26, H24	AD[31:0]	I/O	***PCI Address and Data.*** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.
B25, B24, G22, F24	CBE_[3:0]	I/O	***Bus Command and Byte Enables.*** During the address phase, C/BE_n[3:0] define the Bus Command. During the data phase, C/BE[3:0]_n define the Byte Enables.
C24	FRAME_	I/O	***PCI Frame.*** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.
C25	IRDY_	I/O	***PCI Initiator Ready.*** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
C26	TRDY_	I/O	***PCI Target Ready.*** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
D24	DEVSEL_	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
D25	STOP_	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
G24	PAR	I/O	***PCI Parity.*** This pin is driven to even parity by PCI master over the AD[31:0] and C/BE_n[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
H23	INTA_	I	***PCI INTA_.*** PCI interrupt input A. It connects to PCI INTA_n when normal modes of PCI Interrupts are supported.
F19	INTB_	I	***PCI INTB_.*** PCI interrupt input B. It connects to PCI INTB_n when normal modes of PCI Interrupts are supported.
F20	INTC_	I	***PCI INTC_.*** PCI interrupt input C. It connects to PCI INTC_n when normal modes of PCI Interrupts are supported.
E19	INTD_	I	***PCI INTD_.*** PCI interrupt input D. It connects to PCI INTD_n when normal modes of PCI Interrupts are supported.

- **EXTERNAL SPI/PORT[3-0] Interface (4 PINs)**

PIN No.	Symbol	Type	Description
W21	E_SPI_CS_/GPIO_P3[0]	I/O	***External SPI Chip Select*** ***General-Purpose Input/Output P3[0]***
W22	E_SPI_CLK/GPIO_P3[1]	I/O	***External SPI Clock*** ***General-Purpose Input/Output P3[1]***
Y21	E_SPI_DO/GPIO_P3[2]	I/O	***External SPI Data Ouput*** ***General-Purpose Input/Output P3[2]***
Y22	E_SPI_DI/GPIO_P3[3]	I/O	***External SPI Data Input*** ***General-Purpose Input/Output P3[3]***

- **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
AA13	IOCHCK_	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
AE16, AF16, AD10, AF15, AF14, AE11, AE10, AD12,Y6, AD14, Y4, AA14,	SD[15:0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during

AA16, AC14, Y1, AA7			memory or I/O write cycles.
AE8	IOCHRDY_	I	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
AB8	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AA3, AA1, AB2, AD2,AA2, AD3, AB7, AE5, AC7, AD6, AC2, AE13, AB11, AA12, AB13 AF12, AC3	SA[16:0]	O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AA9, AD5, AB9	SA[19:17]	O	**ISA slot address bus.** ISA slot address bus for 62-pin slot.
AC13	SBHE_	O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
AC15, AD13, AE14, AA15, AD15, AB15, AE9	LA[23:17]	O	**ISA latched address bus**. These are input signal during ISA master cycle.
AF9	MEMR_	O	**ISA memory read**. This signal is an input during ISA master cycle.
AE12	MEMW_	O	**ISA memory write**. This signal is an input during ISA master cycle.
	RST_DRV	O	**Driver Reset**. This output signal is driven active during system power up.
AF4, AF2, AC8, AF3, AE6, AB14, AE7, AC1, AD7, AD1, AE2	IRQ[7:3], IRQ[12:9], IRQ[15:14]	I	**Interrupt request signals**. These are interrupt request input signals.
AE15, AF11, AA11, Y5, AC9, AD4, AB12	DRQ[7:5], DRQ[3:0]	I	**DMA device request**. These are DMA request input signals.
AD8	0WS_	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
AA10	SMEMR_	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
AA8	SMEMW_	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.
Y2	IOW_	O	**ISA I/O write**. This signal is an input during ISA master cycle.
AB16	IOR_	O	**ISA I/O read**. This signal is an input during ISA master cycle.
AF7, AD11, AB10, Y3, AF13, AB3, AD9	DACK_[7:5], DACK_[3:0]	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
AF6	REFRESH_	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AF10	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
AF5	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
AE4	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
AE1	MEMCS16_	I	ISA 16-bit memory device select indicator signal.
AE3	IOCS16_	I	ISA 16-bit I/O device select indicator signal.
AF8	OSC14M	O	14.318MHz clock out

- **Chip Selection Interface (3 PINs)**

PIN No.	Symbol	Type	Description
AC16	GPCS0_	O	**ISA Bus Chip Select 0**. This pin is the chip select for ISA bus.
AD16	GPCS1_	O	**ISA Bus Chip Select 1**. This pin is the chip select for ISA bus.
G21	ROMCS_/SPICS_	O	***ROM Chip Select.*** This pin is used as a ROM chip select. ***SPI Chip Select.*** This pin is used as SPI flash chip select.

- **Redundant (4 PIN)**

PIN No.	Symbol	Type	Description
U21	EXTSYSFAILIN_	I	**External system fail input**. This pin is the system fail in for redundant.
U22	SYSFAILOUT_	O	**System fail output**. This pin is the system fail out for redundant.
V22	EXT_SWITCH_FAIL_	I	**External switch fail**. This pin is the switch input for redundant.
V21	EXT_GPCS_	I	**External GPCS input**. This pin is the GPCS in for redundant.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
V13	KBCLK/KBRST	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042. **Keyboard Reset**. This pin is Keyboard reset when used external 8042.
V16	KBDAT/A20GATE	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042. **Address Bit 20 Mask**. This pin is A20 mask when used external 8042.
V14	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
V15	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

- **RTC/PORT3[7-4] Interface (7 PINs)**

PIN No.	Symbol	Type	Description
N21	RTC_AS /GPIO_P3[7]	I/O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC. ***General-Purpose Input/Output GPIO P3[7].***
P22	RTC_RD_ /GPIO_P3[6]	I/O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC. ***General-Purpose Input/Output GPIO P3[6].***
T21	RTC_WR_ /GPIO_P3[5]	I/O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC. ***General-Purpose Input/Output GPIO P3[5].***
R22	RTC_IRQ8_ /GPIO_P3[4]	I/O	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input. ***General-Purpose Input/Output GPIO P3[4].***
T22	RTC_PS	I	***RTC Battery Power Sense.***
V25	RTC_XOUT	O	***Crystal-out***.
V26	RTC_XIN	I	***Crystal-in.***

- **COM1/PORT4 Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AE21	SIN1/GPIO_P4[4]	I/O	***Receive Data.*** FIFO UART receiver serial data input signal. ***General-Purpose Input/Output GPIO port4 [4].***
AE22	SOUT1/GPIO_P4[1]	I/O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port. ***General-Purpose Input/Output GPIO port4 [1].***
AF22	RTS1/GPIO_P4[2]	I/O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***General-Purpose Input/Output GPIO port4 [2].***

AE23	CTS1/GPIO_P4[7]	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_n.* ***General-Purpose Input/Output GPIO port4 [7].***
AF23	DSR1/GPIO_P4[6]	I/O	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_n.* ***General-Purpose Input/Output GPIO port4 [6].***
AF24	DCD1/GPIO_P4[0]	I/O	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD_n.* ***General-Purpose Input/Output GPIO port4 [0].***
AD22	RI1/GPIO_P4[3]	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). An RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_n.* ***General-Purpose Input/Output GPIO port4 [3].***
AD23	DTR1/GPIO_P4[5]	I/O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***General-Purpose Input/Output GPIO port4 [5].***
AD21	TXD_EN1	I/O	***COM1 TX Status.*** This pin will be high when COM1 is trnamitting.

- **COM2/PWM Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AF25	SIN2/PWM2CLK	I	***COM2 Receive Data.*** FIFO UART receiver serial data input signal. ***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AE24	SOUT2/PWM0OUT	O	***COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port. ***PWM Timer0 Output.*** This pin is PWM timer0 output when SB register C0h bit2 is 1 (PINs for PWM).
AD25	RTS2/PWM1OUT	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AD26	CTS2/PWM1GATE	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_n.* ***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AE26	DSR2/PWM0GATE	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_n.* ***PWM Timer0 Gate.*** This pin is PWM timer0 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AC26	DCD2/PWM0CLK	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD_n.* ***PWM Timer0 Clock.*** This pin is PWM timer0 external clock input when SB register C0h bit2 is 1 (PINs for PWM).

AD24	RI2/PWM1CLK	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). An RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_n.* ***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AC25	DTR2/PWM2OUT	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AE25	TXD_EN2/PWM2GATE	I/O	***COM2 TX Status.*** This pin will be high when COM2 is trnamitting. ***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

- **COM3, 4, 9 (6 PIN)**

PIN No.	Symbol	Type	Description
G3	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
G2	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
N6	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
M6	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
K6	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
J6	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

- **IDE 0, 1/COM3,4,PRINT1 Interface (58 PINs)**

PIN No.	Symbol	Type	Description
K4, K5, L5, M4, K3, M2, L2, K2	PD[7:0]/SDD[7:0]	I/O	***Parallel port data bus bit .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
N5	SLCT/SDD8	I/O	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
L6	PE/SDD9	I/O	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
M5	BUSY/SDD10	I/O	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***

L4	ACK_/SDD11	I/O	***ACK_.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
M3	SLIN_/SDD12	SLIN_: OD SDD12: I/O	***SLIN_.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
J1	INIT_/SDD13	INIT_: OD SDD13: I/O	***INIT_.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
N4	ERR_/SDD14	I/O	***ERR_.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
L3	AFD_/SDD15	AFD_: OD SDD15: I/O	***AFD_.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Data Bus.***
H3	RTS3_/SRST_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***IDE Secondary Channel Reset.***
J2	DCD3_/SDRQ	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD_n.* ***IDE Secondary Channel DMA Request.***
P6	CTS4_/SIOW_	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_n.* ***IDE Secondary Channel IO Write Strobe.***
H2	CTS3_/SIOR_	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_n.* ***IDE Secondary Channel IO Read Strobe.***

G1	RI3/SIORDY	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). An RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_n.* ***IDE Secondary Channel IO Channel Ready.***
F1	DTR3_/SDACK_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***IDE Secondary Channel DMA Acknowledge.***
U6	RTS4_/SINT	I/O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***IDE Secondary Channel Interrupt.***
V5	RI4/SA1	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). An RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_n.* ***IDE Secondary Channel Device Address.***
H1	DSR3_/SCBLID_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_n.* ***IDE Secondary Channel Cable Assembly Type Identifier.***
V6	DTR4_/SA0	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***IDE Secondary Channel Device Address.***
R6	DCD4_/SA2	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD_n.* ***IDE Secondary Channel Device Address.***

L1	STB_/SCS_0	STB_: OD SCC_0: I	***STB_.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. ***IDE Secondary Channel Chip Select.***
T6	DSR4_/SCS1_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_n.* ***IDE Secondary Channel Chip Select.***
M1	PRST_	O	***IDE Primary Channel Reset.***
V2, W2, P1, P5, U5, P4, N3, U3, U4 T4, R4, U2, N1, R5, T5, T3	PDD[15:0]	I/O	***IDE Primary Channel Data Bus.***
R1	PDRQ	I	***IDE Primary Channel DMA Request.***
R3	PIOW_	O	***IDE Primary Channel IO Write Strobe.***
V1	PIOR_	O	***IDE Primary Channel IO Read Strobe.***
P3	PIORDY	I	***IDE Primary Channel IO Channel Ready.***
T1	PDACK_	O	***IDE Primary Channel DMA Acknowledge.***
N2	PINT	I	***IDE Primary Channel Interrupt.***
K1, P2, R2	PA[2:0]	O	***IDE Primary Channel Device Address***
U1	PCBLID_	I	***IDE Primary Channel Cable Assembly Type Identifier.***
W1	PCS0_	O	***IDE Primary Channel Chip Select.***
T2	PCS1_	O	***IDE Primary Channel Chip Select.***

- **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
W24	SERIRQ	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture.
W23, V23, U23, T23	LAD[3:0]	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function.
U18	LFRAME_	O	***Low Pin Count FRAME_n Signal.*** This signal is used as a frame signal of low pin count protocol..
V18	LDRQ_	I	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol.

- **GPIO Interface (24 PINs)**

PIN No.	Symbol	Type	Description
AA18, AA17, AE18, AE17, AF18, AF17, AC17, AD17, AA19, AC19, AD19, AE19, AB18, AC18, AB17, AF19	GPIO_P0[7:0] GPIO_P1[7:0]	I/O	***General-Purpose Input/Output P0[7-0] and P1[7-0].*** Those pins can be programmed input or output individually.
AA20, AB20, AD20, AE20, AD18, AF20, AF21, AB19	GPIO_P2[7:0]/Address[31:24]	I/O	***General-Purpose Input/Output P2[7-0] .*** Those pins can be programmed input or output individually. ***Address[31:24].***

- **Ethernet Interface (24 PINs)**

PIN No.	Symbol	Type	Description
L22	Link/Active		***Link/Active:*** Link/active status
K22	Duplex		***Duplex:*** Duplex status
J24	ISET		***ISET:*** External resistor connecting pin for BIAS
F22	ATSTP		***ATSTP:*** VGA and ADC testing pin for input and output (positive)
F21	ATSTN		***ATSTN:*** VGA and ADC testing pin for input and output (negative)
K25	TXN		***TXN:*** 10B-T/100BT transmitting output pin/ reveiving input pin (positive)
K26	TXP		***TXP:*** 10B-T/100BT transmitting output pin/ reveiving input pin (negative)
L25	RXN		***RXN:*** 10B-T/100BT reveiving input pin/ transmitting output pin (positive)
L26	RXP		***RXP:*** 10B-T/100BT reveiving input pin/ transmitting output pin (negative)
J16	MDC	O	***MDC:*** MII management data clock is sourced by the Vortex86SX to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
K16	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and the Vortex86SX.
L16	COL0	I	***COL0:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
M21	RXC0	I	***RXC0:*** Supports the receive clock supplied by the external PMD device. This clock should always be active.
M18, M17, L17, L18	RXD0_[3:0]	I	***RXD0_[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
L21	RXDV0	I	***RXDV0:*** Data valid is asserted by an external PHY when the received data is present on the RXD[3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
J21	TXC0	I	***TXC0:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
J18, J17, K17, K18	TXD0_[3:0]	O	***TXD0_[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
K21	TXEN0	O	***TXEN0:*** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
G6	TDO	O	***TDO:*** JTAG Test Data Output pin.
J9	TMS	I	***TMS:*** JTAG Test Mode Select pin.
G7	TCK	I	***TCK:*** JTAG Test Clock Input pin.
H6	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **TEST PIN (10 PIN)**

PIN No.	Symbol	Type	Description
J3	TESTCLK	I/O	For Testing used
E23, E21, D22, E22, D23, F2, F3, E2, E3	TEST[8:0]	I/O	For Testing used. Test 3 and Test 4 must pull high to 3.3V.

- **1.2V POWER (14 PINs)**

PIN No.	Symbol	Type	Description
D9, D10	VDDLL (2 PINs)	I	DLL power
E9, E10	GNDDLL (2 PINs)	I	DLL ground
F8,F13,F14,G4, J14,K14,L14,N9 ,M14,P9	VCCK (10 PINs)	I	Core power
E7,E8,E17,J10, J11,J12,K9, K10,K11,K12, L9,L10,L11, L12,M9,M10, M11	GNDK (17 PINs)	I	Code ground

- **1.8V POWER (57 PINs)**

PIN No.	Symbol	Type	Description
C4,C5,C6,C7, D4,D7,D8,E4	VCCO (8 PINs)	I	SDR/DDRII power (3.3V/1.8V)
D5,D6,E5,E6, F4,F5,F6,F7, G5	GNDO (9 PINs)	I	SDR/DDRII gound
AA21,AA22, AA23,AC4, AC5,AC6,T11, T12,U10,V10	Vdd_core (10 PINs)	I	Core power
T16, T17, T18, U11, U12, U13, U14, U15, U16, V4, V11, V12, AB4, AB5, AB6, AC10, AC1, AC12	Vss_core (18 PINs)	I	Core ground
N22, R24, R23, W26	AVDD[3:0]	I	Analog power
N24, P23, T24, W25	AVSS[3:0]	I	Analog gound
N23, V24	AVDDPLL[1:0]	I	USB PLL power
P25, U25	AVSSPLL[1:0]	I	USB PLL ground

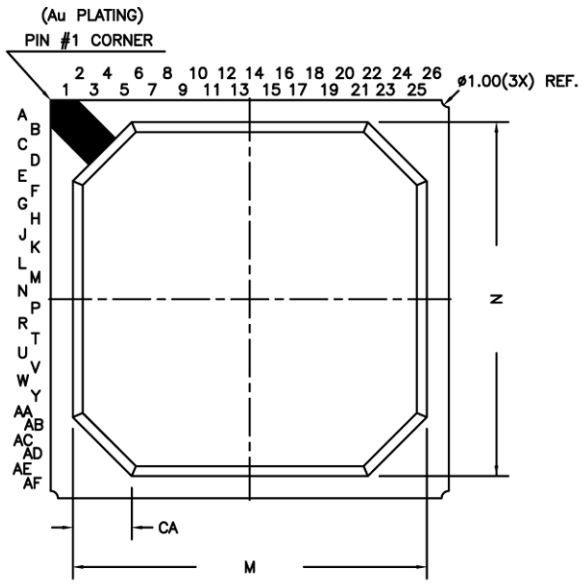
- **Battery POWER (2 PIN)**

PIN No.	Symbol	Type	Description
P21	VBat	I	Battery power for RTC
R21	VBatGnd	I	Battery gound for RTC

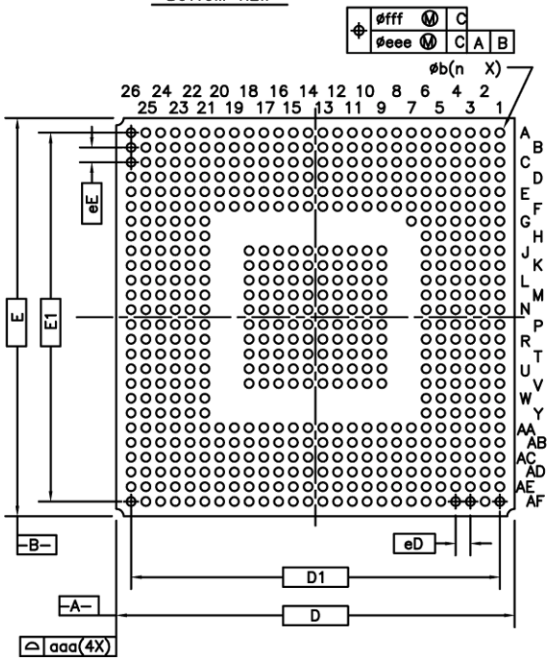
- **3.3V Power (87 PINs)**

PIN No.	Symbol	Type	Description
H4, J4	VPLL (2 PINs)	I	Analog power
H5, J5	GNDPLL (2 PINs)	I	Analog gound
AA24, AB24	Vdd_pll (2 PINs)	I	Analog power
Y24, AC24	Vss_pll (2 PINs)	I	Analog gound
E18, F18, J15, K15, L15, M15, M16, P10, P11, P12, P13, P14	VCC3V (12 PINs)	I	Analog power
F15, F16, F17, J13, K13, L13, M12, M13, N10, N11, N12, N13, N14, N15, N16	GND_R3 (15 PINs)	I	Analog gound
AA4, AA5, AA6, AC21, AC22, AC23, N17, N18, P15, P16, R9, R10, R13, R14, V3, W3, W4	Vdd_io (17 PINs)	I	IO power
P17, P18, R11, R12, R15, R16, R17, R18,T9, T10, T13, T14, T15, U9, U17, V9, V17, W5, W6, AB21, AB22, AB23, AC20	Vss_io (23 PINs)	I	IO gound
K23	VSSAPLL	I	Analog ground
J23	VCCAPLL	I	Analog power
M22	VSSABG	I	Analog gound
M23	VCCABG	I	Analog power
K24	VCCA0	I	Analog power
L23	VSSA0	I	Analog gound
L24	VCCA1	I	Analog power
M24	VSSA1	I	Analog gound
U24	AVDD33_0	I	Analog power
P24	AVDD33_1	I	Analog power
F23	VCC_SPI	I	SPI flash power
D21	GND_SPI (2 PINs)	I	SPI flash ground

TOP VIEW

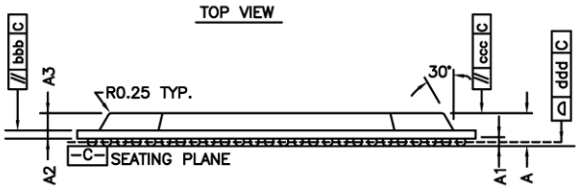


BOTTOM VIEW



		Symbol	Common Dimensions
Package :			PBGA
Body Size:	X	D	27
	Y	E	27
Ball Pitch :	X	eD	1
	Y	eE	1
Total Thickness :		A	2.23 +/- 0.13
Mold Thickness :		A3	1.17 Ref.
Substrate Thickness :		A2	0.56 Ref.
Ball Diameter :			0.60
Stand Off :		A1	0.40~0.60
Width :		b	0.50 ~ 0.70
Mold Area :	X	M	24
	Y	N	24
Chamfer		CA	4
Package Edge Tolerance :		aaa	0.20
Substrate Flatness :		bbb	0.25
Mold Flatness :		ccc	0.35
Coplanarity:		ddd	0.20
Ball Offset (Package) :		eee	0.25
Ball Offset (Ball) :		fff	0.10
Ball Count :		n	581
Edge Ball Center to Center :	X	D1	25
	Y	E1	25

TOP VIEW



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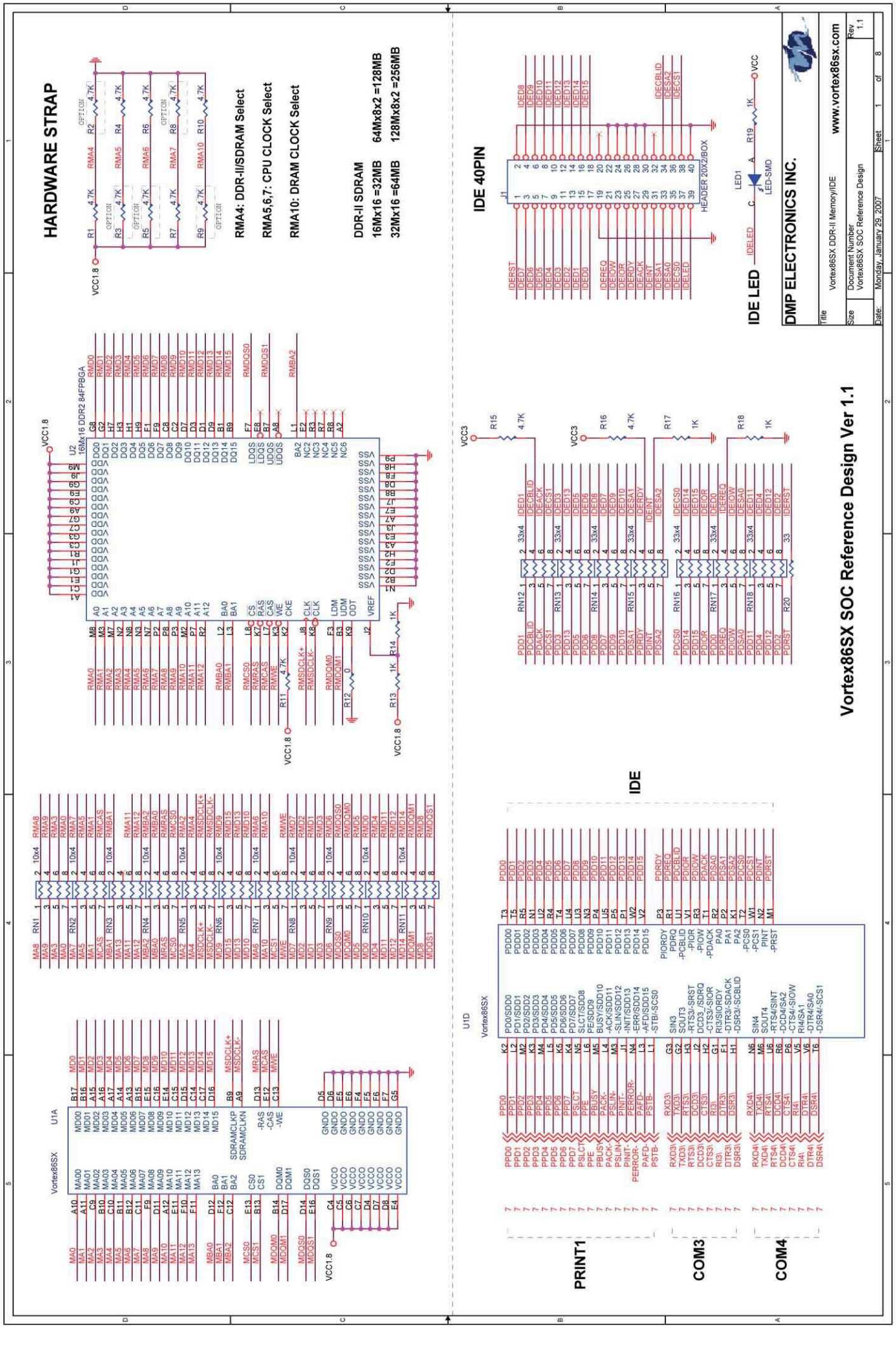
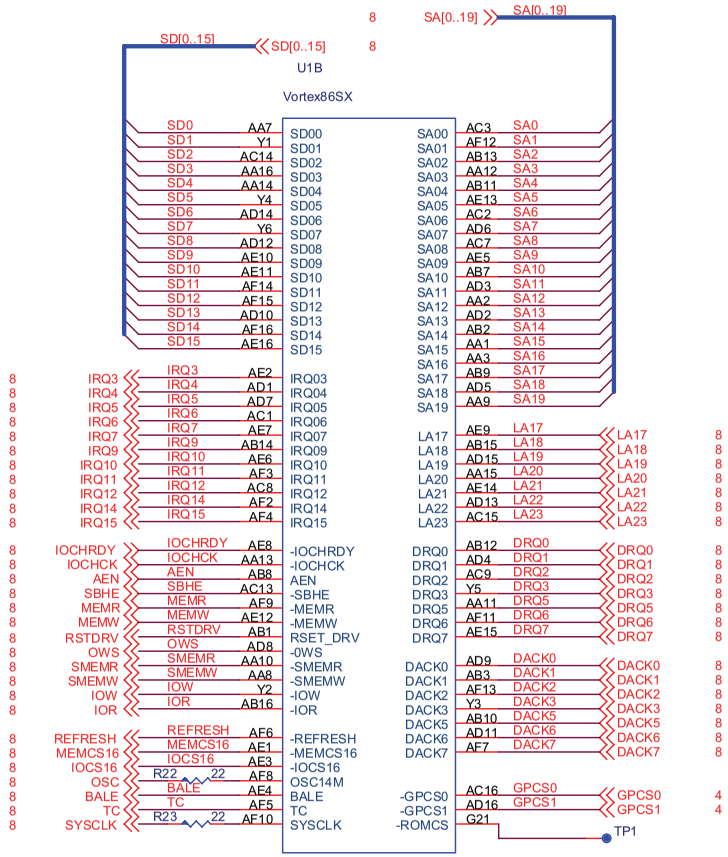
		DWG. NO.: AAA03214	REV.: 0
		SHEET: 1 OF 2	SIZE: A4
UNIT	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: MS-034	

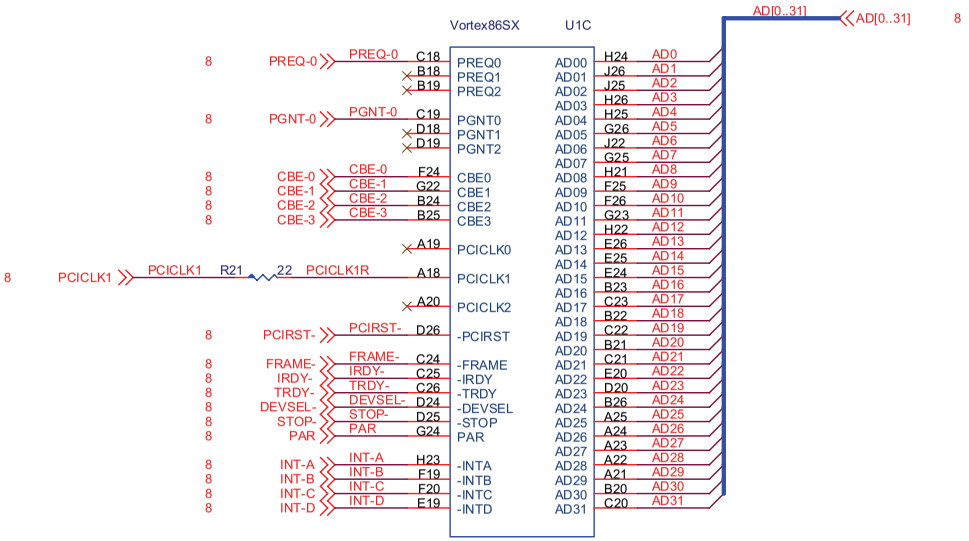
6. Reference Design Schematic



ISA BUS



PCI BUS



DMP ELECTRONICS INC.		
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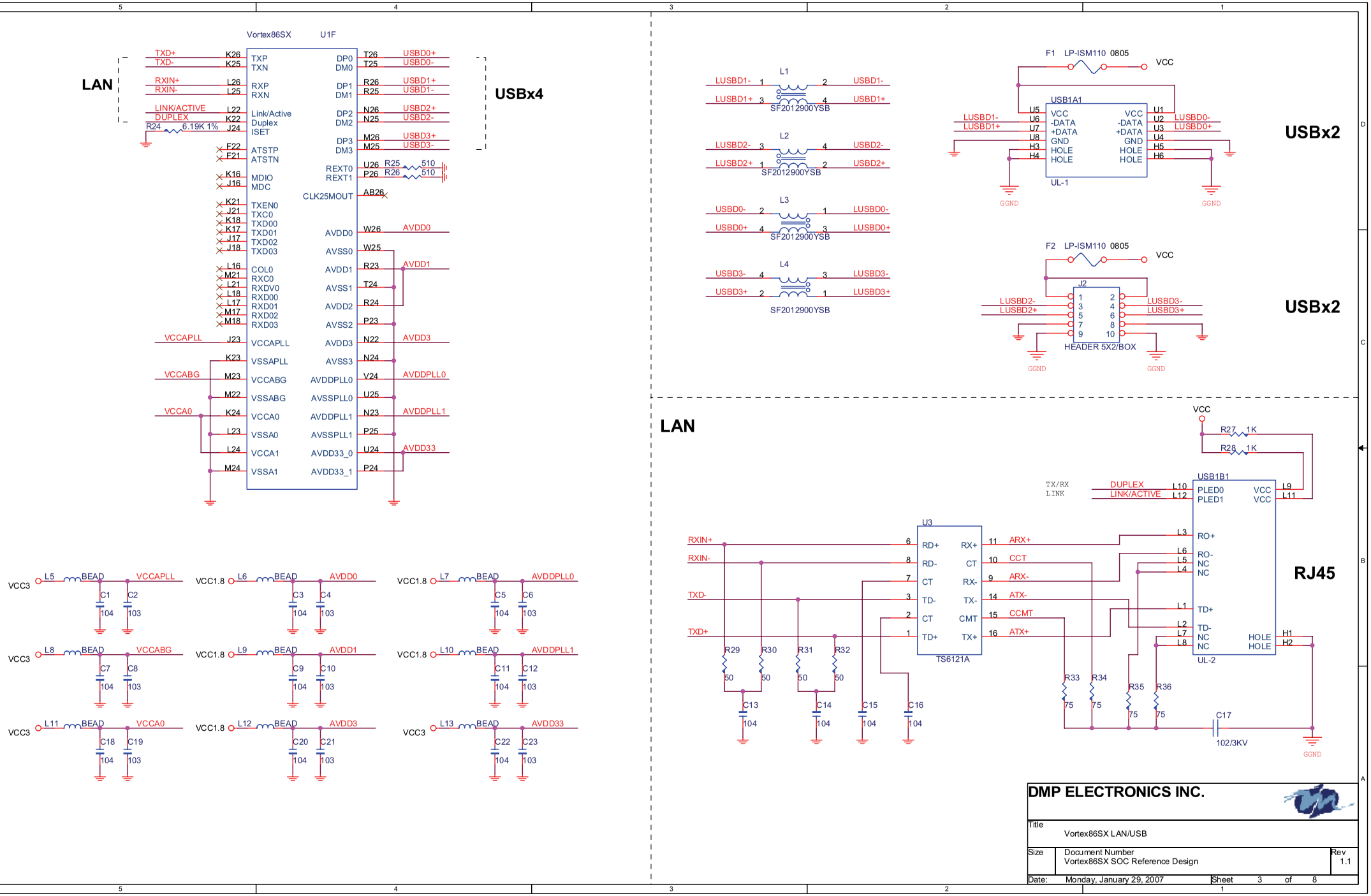
Size	Document Number: Vortex86SX SOC Reference Design	Rev: 1.1
Date: Monday, January 29, 2007	Sheet 2 of 8	


LAN
Vortex86SX U1F
TXD+ K26 TXP
TXD- K25 TXN
RXIN+ L26 RXP
RXIN- L25 RXN
LINK/ACTIVE L22 Link/Active
DUPLEX K22 Duplex
R24 6.19K 1% J24 ISET
F22 ATSTP
F21 ATSTN
K16 MDIO
J16 MDC
K21 TXEN0
J21 TXC0
K18 TXD00
K17 TXD01
J17 TXD02
J18 TXD03
L16 COL0
M21 RXC0
L21 RXDV0
L18 RXD00
L17 RXD01
M17 RXD02
M18 RXD03
VCCAPLL J23 VCCAPLL
K23 VSSAPLL
VCCABG M23 VCCABG
M22 VSSABG
VCCA0 K24 VCCA0
L23 VSSA0
L24 VCCA1
M24 VSSA1
DP0 T26 USBD0+
DM0 T25 USBD0-
DP1 R26 USBD1+
DM1 R25 USBD1-
DP2 N26 USBD2+
DM2 N25 USBD2-
DP3 M26 USBD3+
DM3 M25 USBD3-
REXT0 U26 R25 510
REXT1 P26 R26 510
CLK25MOUT AB26
AVDD0 W26 AVDD0
AVSS0 W25
AVDD1 R23 AVDD1
AVSS1 T24
AVDD2 R24
AVSS2 P23
AVDD3 N22 AVDD3
AVSS3 N24
AVDDPLL0 V24 AVDDPLL0
AVSSPLL0 U25
AVDDPLL1 N23 AVDDPLL1
AVSSPLL1 P25
AVDD33_0 U24 AVDD33
AVDD33_1 P24
USBx4
VCC3 L5 BEAD VCCAPLL C1 104 C2 103
VCC1.8 L6 BEAD AVDD0 C3 104 C4 103
VCC1.8 L7 BEAD AVDDPLL0 C5 104 C6 103
VCC3 L8 BEAD VCCABG C7 104 C8 103
VCC1.8 L9 BEAD AVDD1 C9 104 C10 103
VCC1.8 L10 BEAD AVDDPLL1 C11 104 C12 103
VCC3 L11 BEAD VCCA0 C18 104 C19 103
VCC1.8 L12 BEAD AVDD3 C20 104 C21 103
VCC3 L13 BEAD AVDD33 C22 104 C23 103
L1 LUSBD1- 1 2 USBD1-
LUSBD1+ 3 4 USBD1+
SF2012900YSB
L2 LUSBD2- 3 4 USBD2-
LUSBD2+ 1 2 USBD2+
SF2012900YSB
L3 USBD0- 2 1 LUSBD0-
USBD0+ 4 3 LUSBD0+
SF2012900YSB
L4 USBD3- 4 3 LUSBD3-
USBD3+ 2 1 LUSBD3+
SF2012900YSB
F1 LP-ISM110 0805
VCC
USB1A1
LUSBD1- U5 VCC VCC U1
LUSBD1+ U6 -DATA -DATA U2 LUSBD0-
U7 +DATA +DATA U3 LUSBD0+
U8 GND GND U4
H3 HOLE HOLE H5
H4 HOLE HOLE H6
UL-1
GGND
USBx2
F2 LP-ISM110 0805
VCC
J2
LUSBD2- 1 2
3 4 LUSBD3-
LUSBD2+ 5 6 LUSBD3+
7 8
9 10
HEADER 5X2/BOX
GGND
USBx2
LAN
VCC
R27 1K
R28 1K
USB1B1
TX/RX LINK
DUPLEX L10 PLED0 VCC L9
LINK/ACTIVE L12 PLED1 VCC L11
U3
RXIN+ 6 RD+ RX+ 11 ARX+
RXIN- 8 RD- CT 10 CCT
7 CT RX- 9 ARX-
TXD- 3 TD- TX- 14 ATX-
2 CT CMT 15 CCMT
TXD+ 1 TD+ TX+ 16 ATX+
TS6121A
R29 50
R30 50
R31 50
R32 50
C13 104
C14 104
C15 104
C16 104
L3 RO+
L6 RO-
L5 NC
L4 NC
L1 TD+
L2 TD-
L7 NC HOLE H1
L8 NC HOLE H2
UL-2
R33 75
R34 75
R35 75
R36 75
C17 102/3KV
GGND
RJ45
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Title
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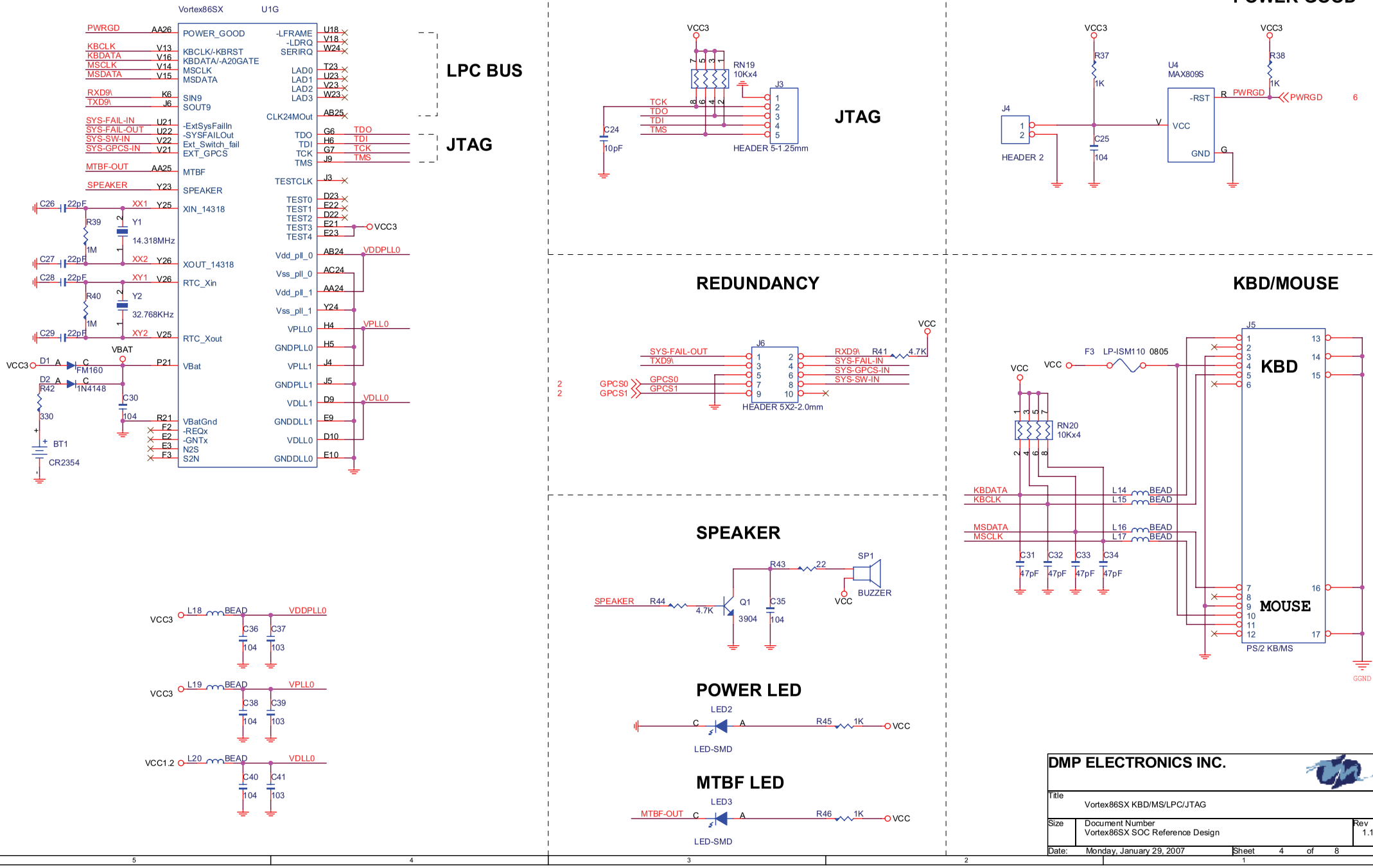
Vortex86SX U1G
LPC BUS
JTAG
REDUNDANCY
POWER GOOD
KBD/MOUSE
SPEAKER
POWER LED
MTBF LED
KBD
MOUSE
PS/2 KB/MS
DMP ELECTRONICS INC.
Vortex86SX KBD/MS/LPC/JTAG
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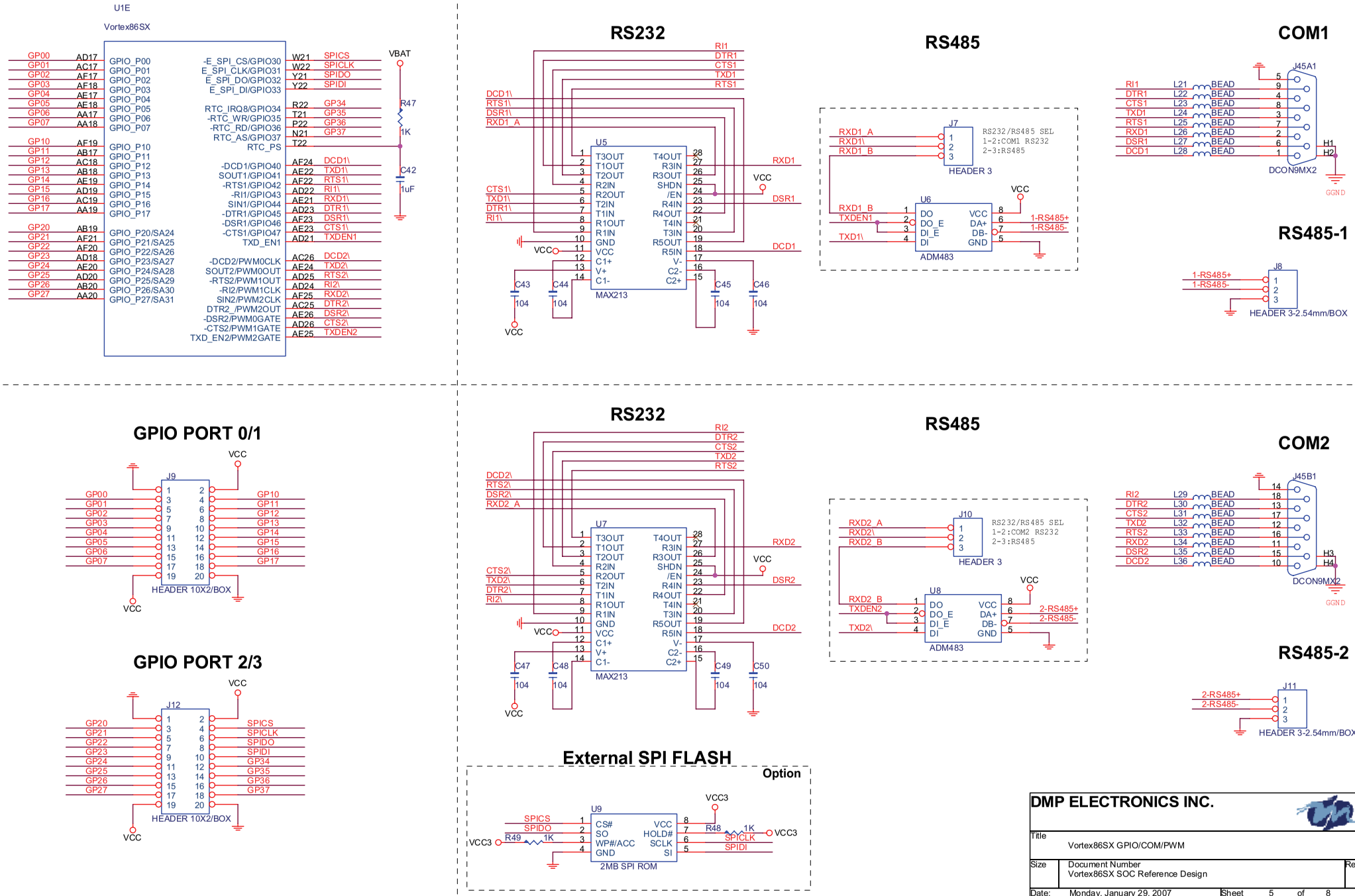
U1E
Vortex86SX
GPIO_P00
GPIO_P01
GPIO_P02
GPIO_P03
GPIO_P04
GPIO_P05
GPIO_P06
GPIO_P07
GPIO_P10
GPIO_P11
GPIO_P12
GPIO_P13
GPIO_P14
GPIO_P15
GPIO_P16
GPIO_P17
GPIO_P20/SA24
GPIO_P21/SA25
GPIO_P22/SA26
GPIO_P23/SA27
GPIO_P24/SA28
GPIO_P25/SA29
GPIO_P26/SA30
GPIO_P27/SA31
-E_SPI_CS/GPIO30
E_SPI_CLK/GPIO31
E_SPI_DO/GPIO32
E_SPI_DI/GPIO33
RTC_IRQ8/GPIO34
-RTC_WR/GPIO35
-RTC_RD/GPIO36
RTC_AS/GPIO37
RTC_PS
-DCD1/GPIO40
SOUT1/GPIO41
-RTS1/GPIO42
-RI1/GPIO43
SIN1/GPIO44
-DTR1/GPIO45
-DSR1/GPIO46
-CTS1/GPIO47
TXD_EN1
-DCD2/PWM0CLK
SOUT2/PWM0OUT
-RTS2/PWM1OUT
-RI2/PWM1CLK
SIN2/PWM2CLK
DTR2_/PWM2OUT
-DSR2/PWM0GATE
-CTS2/PWM1GATE
TXD_EN2/PWM2GATE
VBAT
R47
1K
C42
1uF
RS232
U5
MAX213
RS485
J7
HEADER 3
U6
ADM483
COM1
J45A1
DCON9MX2
RS485-1
J8
HEADER 3-2.54mm/BOX
GPIO PORT 0/1
J9
HEADER 10X2/BOX
GPIO PORT 2/3
J12
HEADER 10X2/BOX
RS232
U7
MAX213
RS485
J10
HEADER 3
U8
ADM483
COM2
J45B1
DCON9MX2
RS485-2
J11
HEADER 3-2.54mm/BOX
External SPI FLASH
Option
U9
2MB SPI ROM
DMP ELECTRONICS INC.
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Vortex86SX GPIO/COM/PWM
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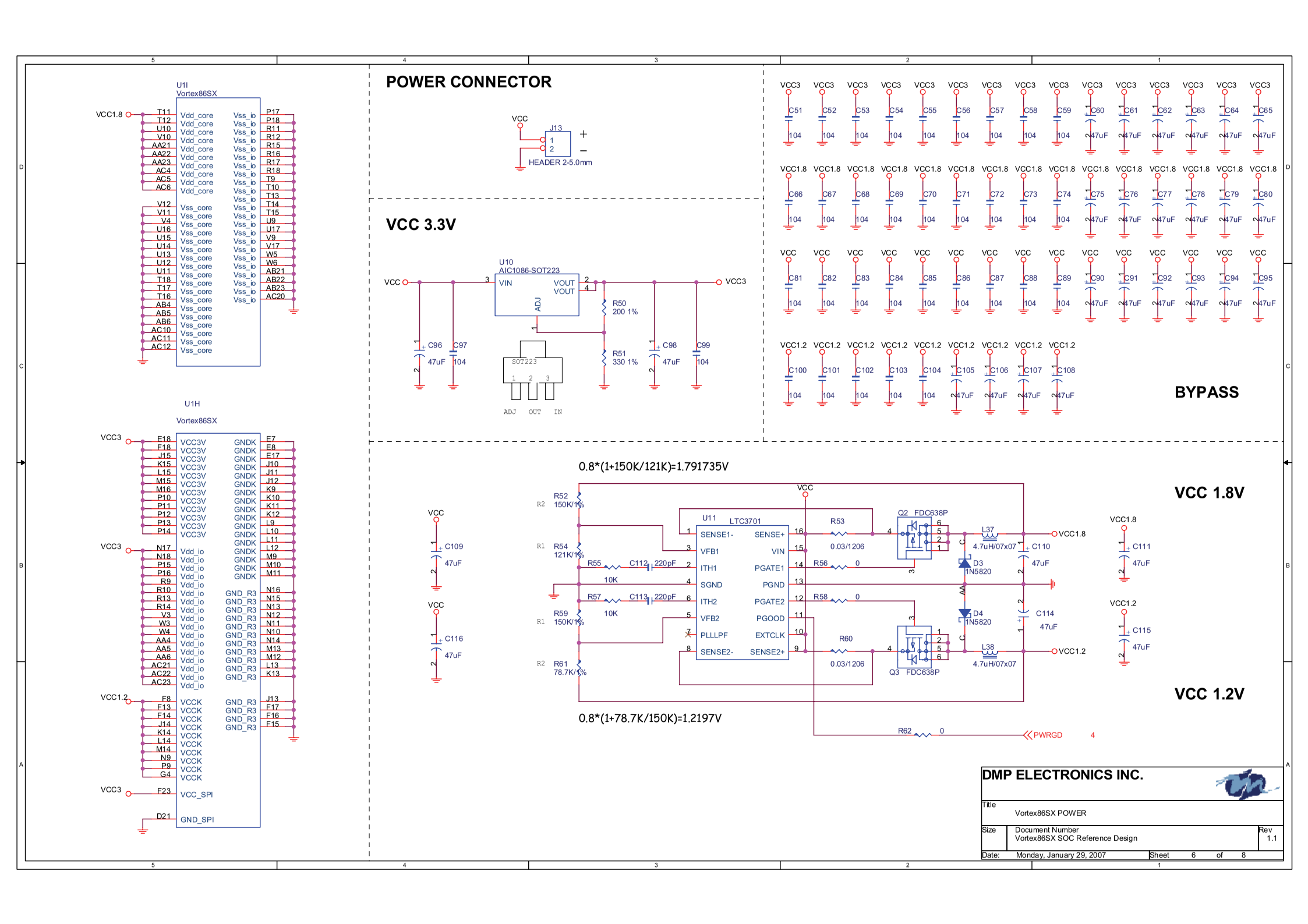
POWER CONNECTOR
VCC
J13
1
2
+
–
HEADER 2-5.0mm
VCC 3.3V
U10
AIC1086-SOT223
VCC
VIN
VOUT
VOUT
ADJ
VCC3
R50
200 1%
R51
330 1%
C96
47uF
C97
104
C98
47uF
C99
104
SOT223
ADJ OUT IN
BYPASS
VCC1.8
VCC1.2
VCC3
C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65
C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80
C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95
C100 C101 C102 C103 C104 C105 C106 C107 C108
104
47uF
U1I
Vortex86SX
VCC1.8
Vdd_core
Vss_core
Vss_io
U1H
Vortex86SX
VCC3
VCC3V
GNDK
VCCK
GND_R3
VCC_SPI
GND_SPI
VCC1.2
0.8*(1+150K/121K)=1.791735V
0.8*(1+78.7K/150K)=1.2197V
VCC 1.8V
VCC 1.2V
U11
LTC3701
SENSE1-
SENSE+
VFB1
VIN
ITH1
PGATE1
SGND
PGND
ITH2
PGATE2
VFB2
PGOOD
PLLLPF
EXTCLK
SENSE2-
SENSE2+
R52
150K/1%
R54
121K/1%
R55
10K
C112
220pF
R57
10K
C113
220pF
R59
150K/1%
R61
78.7K/1%
R53
0.03/1206
R56
0
R58
0
R60
0.03/1206
R62
0
Q2 FDC638P
Q3 FDC638P
L37
4.7uH/07x07
L38
4.7uH/07x07
D3
1N5820
D4
1N5820
C109
47uF
C116
47uF
C110
47uF
C111
47uF
C114
47uF
C115
47uF
PWRGD
4
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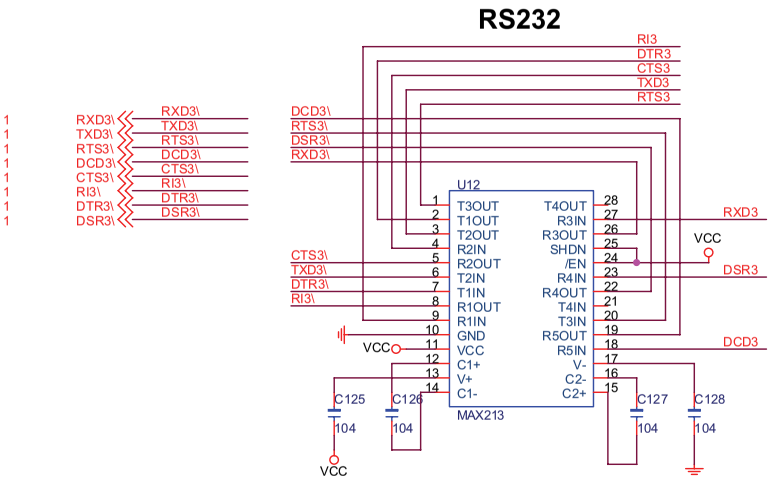
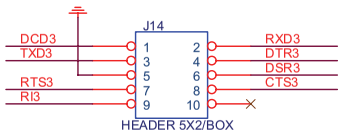
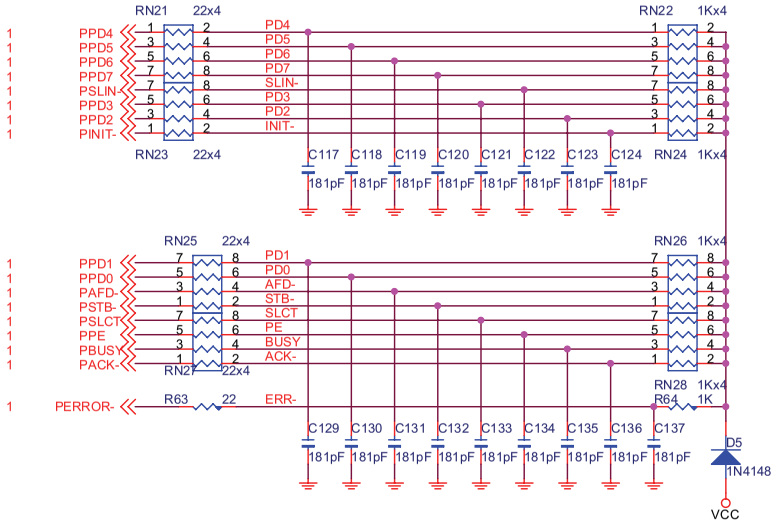
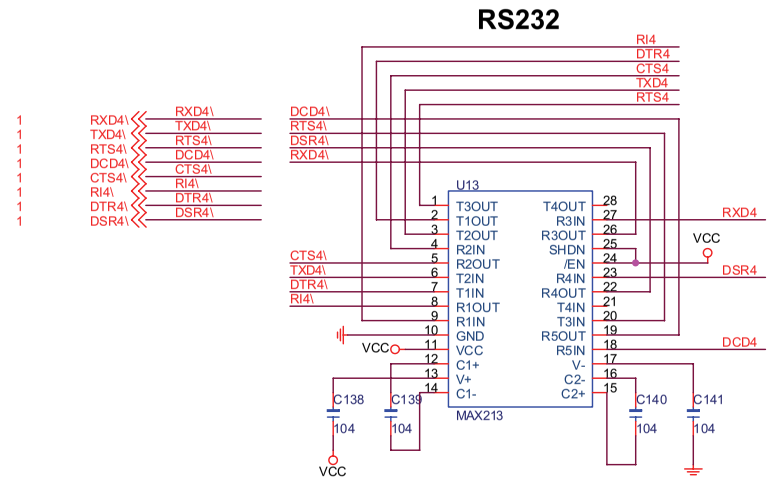
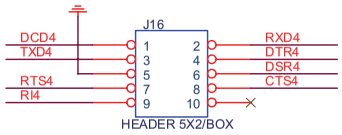
PRINT1/COM3/COM4

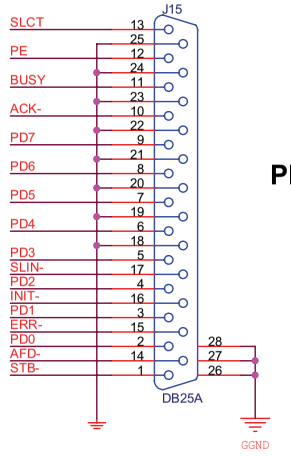












PRINT1

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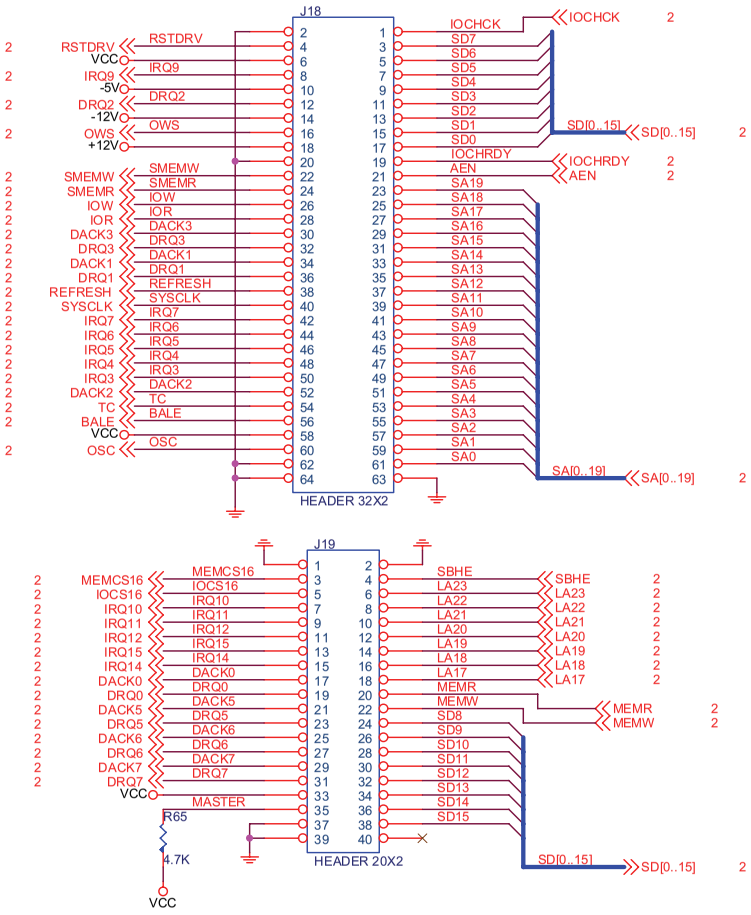
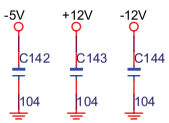
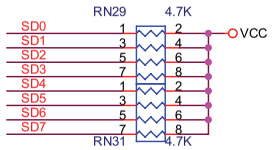
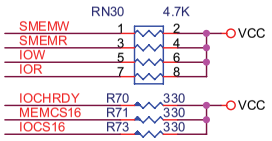
PC-104 / Full 16Bit ISA BUS

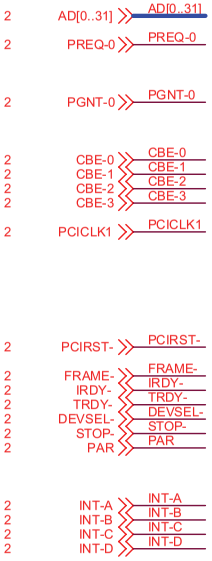




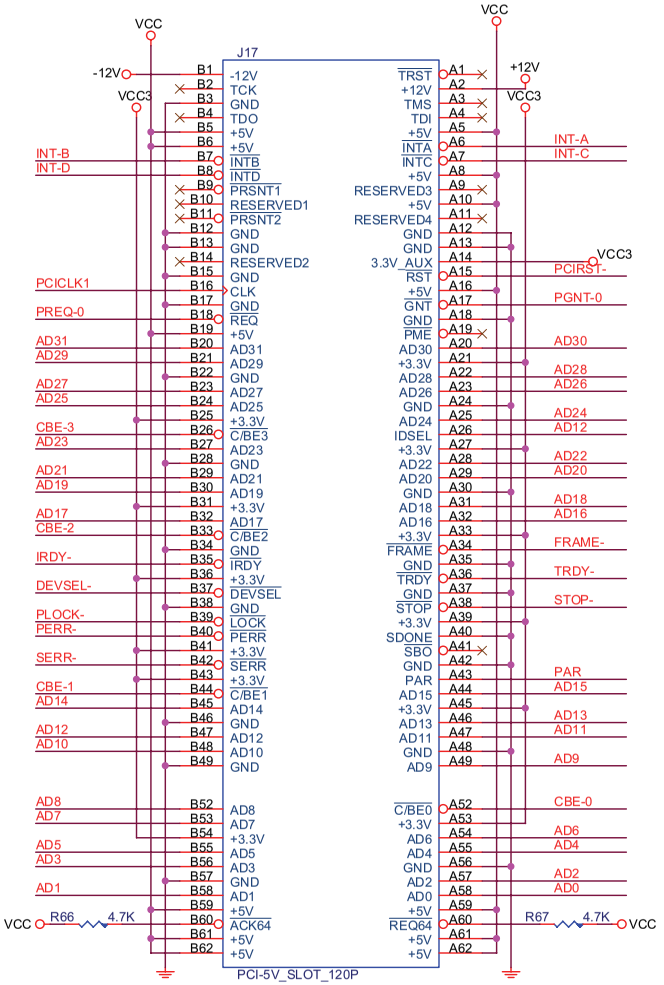


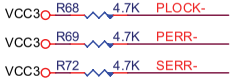


PCI BUS



PCI SLOT





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