1. Overview

The **Vortex86MX** is a high performance and fully static 32-bit x86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, 256KB write through/write back 4-way L2 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, DDR2, ROM controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE controller within a single 720-pin BGA package to form a system-on-a-chip **(SOC)**. It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC to bring about desired performance.

2. Features

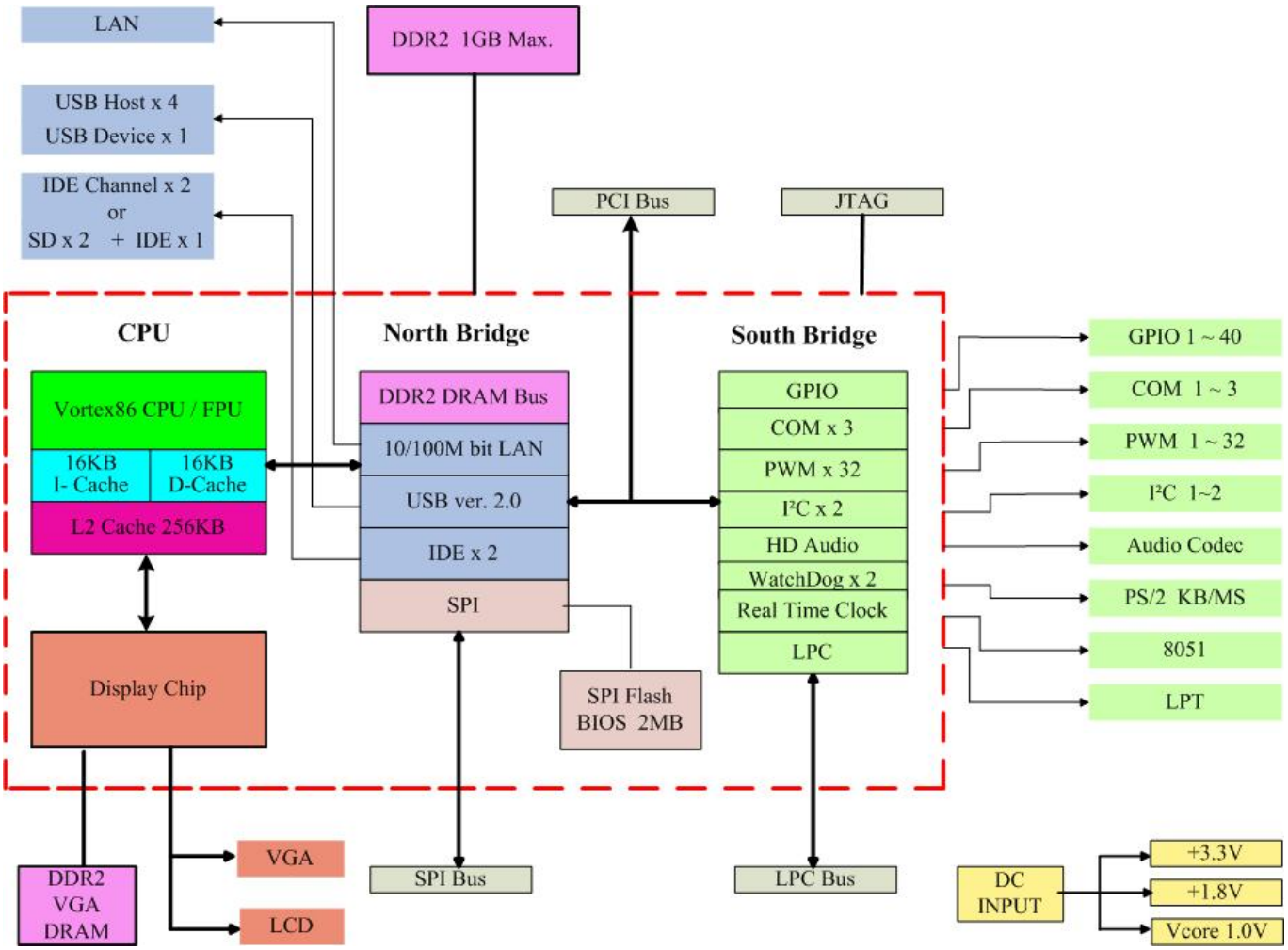
- **X86 Processor Core**
  - 6-stage pipeline
- **Floating point unit support**
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-wary 256KB L2 Cache
  - Write through or write back policy
- **DDRII Control Interface**
  - 16 bits data bus
  - DDRII clock support up to 400MHz
  - DDRII size support up to 1Gbytes
- **IDE Controller**
  - Supports 2 channels Ultra-DMA 100 (Disk x 4)
  - Primary channel support SD card
- **LPC (Low Pin Count) Bus Interface**
- **GPU Control Unit**
  - VGA controller
  - 2D Graphics engine support
- **MAC Controller x 1**
- **PCI Control Interface**
  - Up to 3 sets PCI master device
  - 3.3V I / O
- **HDA Controller**
- **DMA Controller**
- **Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- **Real Time Clock**
  - Less than 2uA (3.0V) power comsuption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 3 (3 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port x 1**
  - Supports SPP/EPP/ECP mode
- **General Programmable I/O**
  - Supports 40 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P4 can be program by 8051
  - GPIO_P0 and GPIO_P1 with interrupt support

(input/output)

- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 4 port
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **Speaker out**
- **Embedded 2MB Flash**
  - For BIOS storage
- **I^2C bus x 2**
  - Compliant w/t V2.1 (not support specific mater code , for example general call, START and CBUS.
- **Servo Control interface support**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 14.318 MHz
  - 32.768 KHz
- **Output clock**
  - 24 MHz
  - 25 MHz
  - PCI clock
  - DDRII clock
- **Operating Voltage Range**
  - Core voltage: 1.0 V ± 5%
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - 0℃ ~ 60℃
- **Package Type**
  - 31x31, 720 Ball BGA

3. Block Diagram

3.1. System Block Diagram



3.2. Functions Block Diagram